CE1901 LABORATORY PROJECT

SUMMARY

In the 1960s, the integrated circuit started a new era in digital design because multiple transistor switches were now integrated together in an enclosed package called a "chip." This integration allowed computers to shrink in size and helped spark the race to outer space, the desktop calculator and eventually the personal computer revolution. Integrated transistor density has followed Moore's law throughout history. Moore's law states that the number of transistors fabricated on chip will double every eighteen months. Table 1 shows the effect of this remarkable doubling law.

Table 1: The Growth of Integration Density

DEVICE CATEGORY	NUMBER OF TRANSISTORS	NUMBER OF LOGIC GATES	DECADE
Small Scale Integration (SSI)	10s	Just a few	mid-1960s
Medium Scale Integration (MSI)	100s	10 – 100	late-1960s
Large Scale Integration (LSI)	1000s	1,000 – 10,000	1970s
Very Large Scale Integration (VLSI)	100,000s	10,000 – 100,000	early-1980s
Ultra Large Scale Integration (ULSI)	1,000,000s+	100,000+	mid-1980s

As the number of devices fabricated on chip continues to grow according to Moore's Law, distinctions by acronym have become uncommon. Today, we routinely fabricate chips with billions of transistors but most people simply state that we are in the VLSI technology era.

While modern digital logic design practice relies extensively on computer-aided design tools and VLSI field-programmable gate arrays (FPGAs) that contain tens-of-thousands of configurable logic components, simpler digital logic chips still play a modest role in digital design. These SSI and MSI chips are used in some system level designs as "glue logic" that helps interface input devices, output devices, and memory systems to the microprocessors that form the heart of modern computing. And, because engineers optimize speed, size, power, and cost, some designs don't warrant the expense of FPGAs, microprocessors, or custom chips.

Thus, it is important that all electrical and computer engineering students know gate-level logic chips from the two historical standards. Texas Instruments created a standard family of chips called the 7400 family. RCA created a standard family of chips called the 4000 family. Each of these families provides a wide range of gates, arithmetic circuits, and other logic functions. Table 2 lists example chips from the 7400 and 4000 families. Every integrated circuit chip is identified in the industry by a unique part number. Engineering students slowly memorize the part numbers as they complete product designs in their undergraduate classes. Note that the

number of gates on the chip is given as part of the function name. Thus, a hex inverter chip has six inverters while a quad 2-input NOR chip has four 2-input NOR gates.

Table 2: Example Logic Gates from the Standard Logic Families

FUNCTION	ACRONYM	7400 SERIES CHIP	4000 SERIES CHIP
Quad 2-input NAND gates	NAND2	7400	4011
Quad 2-input NOR gates	NOR2	7402	4001
Hex Inverter	NOT	7404	4049
Quad 2-input AND gates	AND2	7408	4081
Quad 2-input OR gates	OR2	7432	4071
AND-OR-INVERT gates	AOI		

Over the next few weeks, students will use their FPGA boards during preliminary laboratory exercises and then use SSI/MSI chips from the standard logic families during in-lab build-wire-test exercises. This will allow you to continue refining your modern FPGA skills while also becoming familiar with the standard pin-outs of the 7400 family of chips. You will also learn to use a waveform pattern generator to apply test voltages to your circuits. And, you will learn to use a logic analyzer to verify that applied test voltages produce correct output voltages.

PRELABORATORY WORK

1. **Design** the canonical circuit for a 3-bit palindrome identifier for non-zero unsigned numbers. A palindrome is a number that is identical when written left-to-right or right-to-left. **Draw** the Quartus schematic. **Simulate** to ensure correct operation.
2. **Design** the canonical circuit for a 3-bit circuit that identifies when two identical outside voltage bits differ from the middle voltage bit. **Draw** the Quartus schematic. **Simulate** to ensure correct operation.
3. **Design** the canonical equation for the 2-bit XOR function. Because the set of gates AND, OR, and NOT is functionally complete, the XOR gate can be built from these gates. **Draw** the Quartus schematic. **Simulate** to ensure correct operation. **Hint:** this problem is no different that problem 1 or 2. Start with the truth table, identify logic-1 rows, write the equation using only AND, OR, and NOT gates.

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DELIVERABLES DUE DURING THE LABORATORY PERIOD

Complete these exercises during the laboratory period.

1. **Demonstrate** your pre-laboratory Quartus schematics and simulations.
2. **Work** this laboratory by yourself.
3. **Use** your CE1901 lab kit or **check out** one set of equipment per team from EECS Tech Support.

Table 3: Required EECS Tech Support Equipment

ITEM	QUANTITY
74LS04 Hex Invert	1
74LS11 Triple 3-input AND	1
74LS32 Quad 2-input OR	1
74LS51 And-Or-Invert	1
Blue Wire Kit	1
Analog Discovery Kit	1
Circuit Design Breadboard with red and blue power strips	1

4. **Build-wire-test** the 3-bit palindrome identifier. **Use** the 74LS04, the 74LS11, and the 74LS32 ICs.
5. **Build-wire-test** the 3-bit outside-middle identifier. **Use** the 74LS04 and the 74LS51 ICs.
6. **Build-wire-test** the 2-bit XOR function. **Use** the 74LS04 and the 74LS51 ICs.
7. **Document** your work in a short laboratory report. **Include** these sections for each problem.
    a. Problem statement
    b. Truth table
    c. Canonical equation
    d. Quartus schematic
    e. Quartus waveform simulation
    f. Analog Discovery Test waveforms